

REMARKS

Claims **1-25** are pending. Reconsideration and timely withdrawal of the pending rejections are requested for the reasons discussed below.

**35 U.S.C. § 102(e) Rejection**

Claims 1, 10-16 and 18-25 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 7,254,231 to VAN DYKE et al. Applicant respectfully traverses this rejection.

The Examiner asserted that VAN DYKE discloses all the features recited in these claims including, among other features, a combinational logic comprising logic functions whose outputs depend solely on their inputs and utilizing logic circuits without memory.

Applicant respectfully disagrees. Notwithstanding the Office Action assertions as to what VAN DYKE discloses, Applicant submits that VAN DYKE fails to disclose, or even suggest at least the features of claims 1, 16, 19 and 21.

In particular, independent claims 1, 16, 19 and 21 recite:

... the combinational logic comprising logic functions whose outputs depend solely on their inputs and utilizing logic circuits without memory.

Applicant does not dispute that VAN DYKE discloses a cryptographic processor which utilizes a DES algorithm (see col. 2, lines 51-67). However, the Examiner is not correct that the general processor (which utilizes ALUs 302, 304 and 306) of VAN DYKE, discussed on col. 4, lines 5-29 and col. 5, line 58 to col. 6, line 2, can be

properly characterized as the recited combinational logic comprising logic functions whose outputs depend solely on their inputs and utilizing logic circuits without memory.

It is clear from the very language cited by the Examiner that the general processor includes pipe line stage 37 which is described as a memory stage. Indeed, Fig. 3 and col. 5, lines 1-12 clearly explains that the memory stage 37 utilizes a conventional cache 312.

As general processor 302/304/306 utilizes memory stage 37, the Examiner is not correct that such a device can be properly characterized as the recited combinational logic comprising logic functions whose outputs depend solely on their inputs and utilizing logic circuits without memory.

The Examiner responds to Applicant's arguments on page 3 of the Final Office Action by explaining that the "shifter" forms part of the recited combinational logic. Such a position, however, ignores the language of col. 5, lines 3-12 of VAN DYKE which clearly states that the output values are generated at memory access pipeline stage 37. Since Fig. 3 of VAN DYKE shows the shifter 314 in memory stage 37, the shifter 314 cannot be properly interpreted as the recited the recited combinational logic comprising logic functions whose outputs depend solely on their inputs and utilizing logic circuits without memory.

Applicant reminds the Examiner that the "broadest reasonable interpretation" standard must be one that "would be understood by one of ordinary skill in the art, taking into consideration the description of the applicant's

specification. *In re Morris*, 127 F.3D 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997)". See page 3 of the previously submitted non-precedential decision *Ex parte HADDAD*. Since Applicant has clearly recited a combinational logic comprising logic functions whose outputs depend solely on their inputs and utilizing logic circuits without memory and consistently argued that the claims do not encompass the disclosed features of VAN DYKE, the Examiner cannot, consistent with *In re Morris*, properly construe these clearly recited features in a manner which is clearly inconsistent with and/or outside the scope of Applicant's specification.

Furthermore, to the extent that the Examiner is basing the instant rejection on an argument of inherency consistent with MPEP 2112, Applicant notes that MPEP 2112 specifically states, in part:

"In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." *Ex parte Levy*, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original) (Applicant's invention was directed to a biaxially oriented, flexible dilation catheter balloon (a tube which expands upon inflation) used, for example, in clearing the blood vessels of heart patients). The examiner applied a U.S. patent to Schjeldahl which disclosed injection molding a tubular preform and then injecting air into the preform to expand it against a mold (blow molding). The reference did not directly state that the end product balloon was biaxially oriented. It did disclose that the balloon was "formed from a thin flexible inelastic, high tensile strength, biaxially oriented synthetic plastic material." *Id.* at 1462 (emphasis in original). The examiner argued that Schjeldahl's balloon was inherently biaxially oriented. The Board reversed on the basis that the examiner did not provide objective evidence or cogent technical reasoning to support the conclusion of inherency.

The Examiner has neither stated that the rejection is based on inherency, nor provided any basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art.

Thus, Applicant submits that independent claims 1, 16, 19 and 21 are not anticipated by any proper reading of VAN DYKE. Furthermore, Applicant submits that dependent claims 10-15, 18, 20 and 22-25 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention.

Applicant requests that the Examiner reconsider and withdraw the rejection of the above-noted claims under 35 U.S.C. § 102(e).

### **35 U.S.C. § 103 Rejection**

Claims 2-9 and 17 were rejected under 35 U.S.C. § 103(a) for being allegedly unpatentable over VAN DYKE in view of US Patent No. 6,704,871 to KAPLAN et al. This rejection is respectfully traversed.

The Examiner acknowledges that VAN DYKE fails to disclose, among other things, the features recited in the above-noted dependent claims. However, the Examiner explains that such features are taught in KAPLAN, and that it would have been obvious to combine the teachings of these documents. Applicant respectfully submits that a *prima facie* case of obviousness has not been established as the applied references fail to teach each and every element of the claims.

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In addition to the arguments noted above regarding VAN DYKE, Applicant submits that this rejection is improper at least because KAPLAN fails to cure the deficiencies of VAN DYKE.

Applicant does not dispute that KAPLAN discloses a cryptographic co-processor having cryptographic function elements (see Abstract). However, KAPLAN, like VAN DYKE, fails to teach a combinational logic comprising logic functions whose outputs depend solely on their inputs and utilizing logic circuits without memory. Indeed, the Examiner has acknowledged as much by withdrawing the anticipation rejection based on KAPLAN.

As VAN DYKE and KAPLAN fail to disclose or suggest at least the features of claims 1 and 16, no proper combination of these documents can possibly render dependent claims 2-9 and 17 unpatentable.

Accordingly, Applicant requests that the Examiner reconsider and withdraw the above-noted rejection under 35 U.S.C. § 103(a) and indicate that these claims are allowable over the applied art of record.

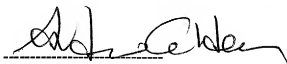
### **CONCLUSION**

In view of the foregoing remarks, Applicant submits that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed.

Please charge any deficiencies in fees and credit any overpayment of fees to

**IBM Deposit Account 50-0563.**

Respectfully submitted,  
J. L. CALVIGNAC et al.

A handwritten signature in black ink, appearing to read 'Andrew M. Calderon', written over a horizontal line.

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